

இந்த கட்டம் "கட்ட வினாக்கள்

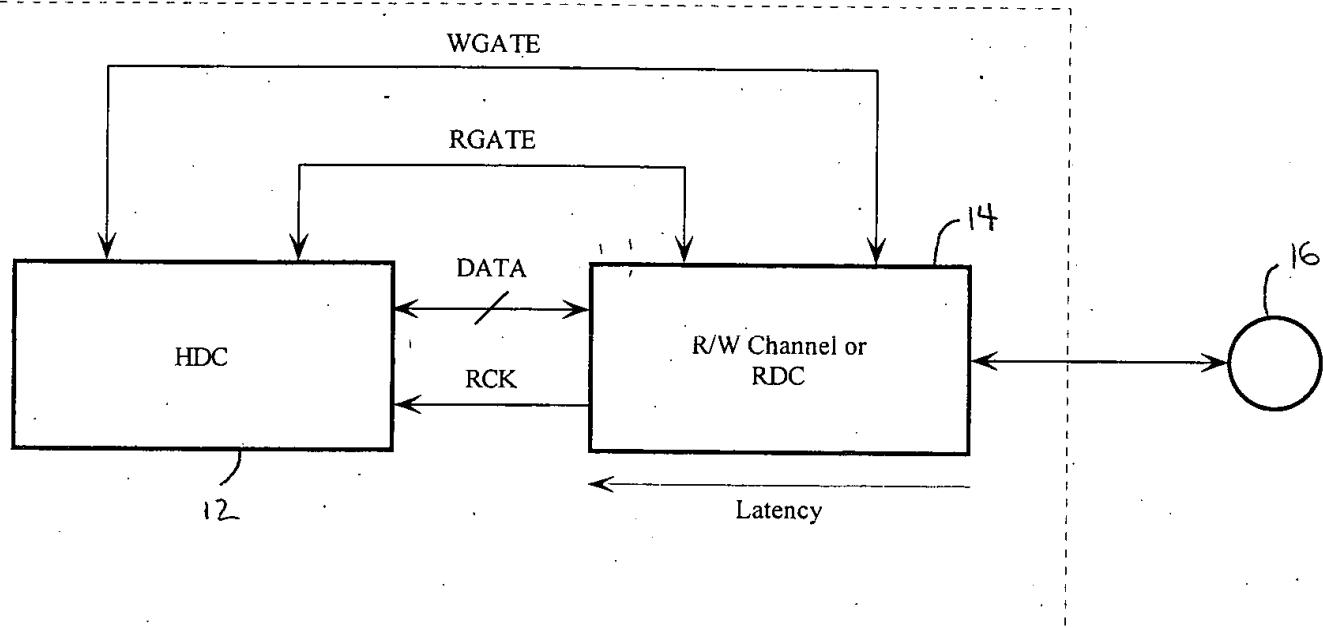


Fig. 1

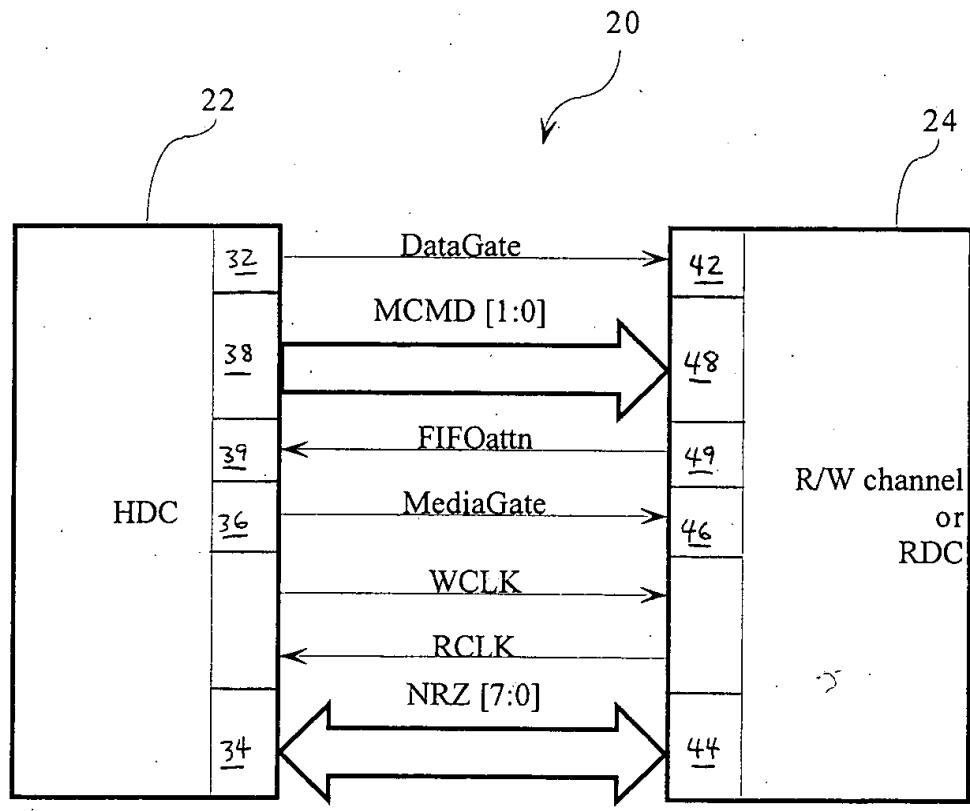


Fig. 2

**MV Interface Description**

This interface uses additional pins to provide Tag/mode selection info for future implementations of high latency RDC designs with latency could be more than one sector long

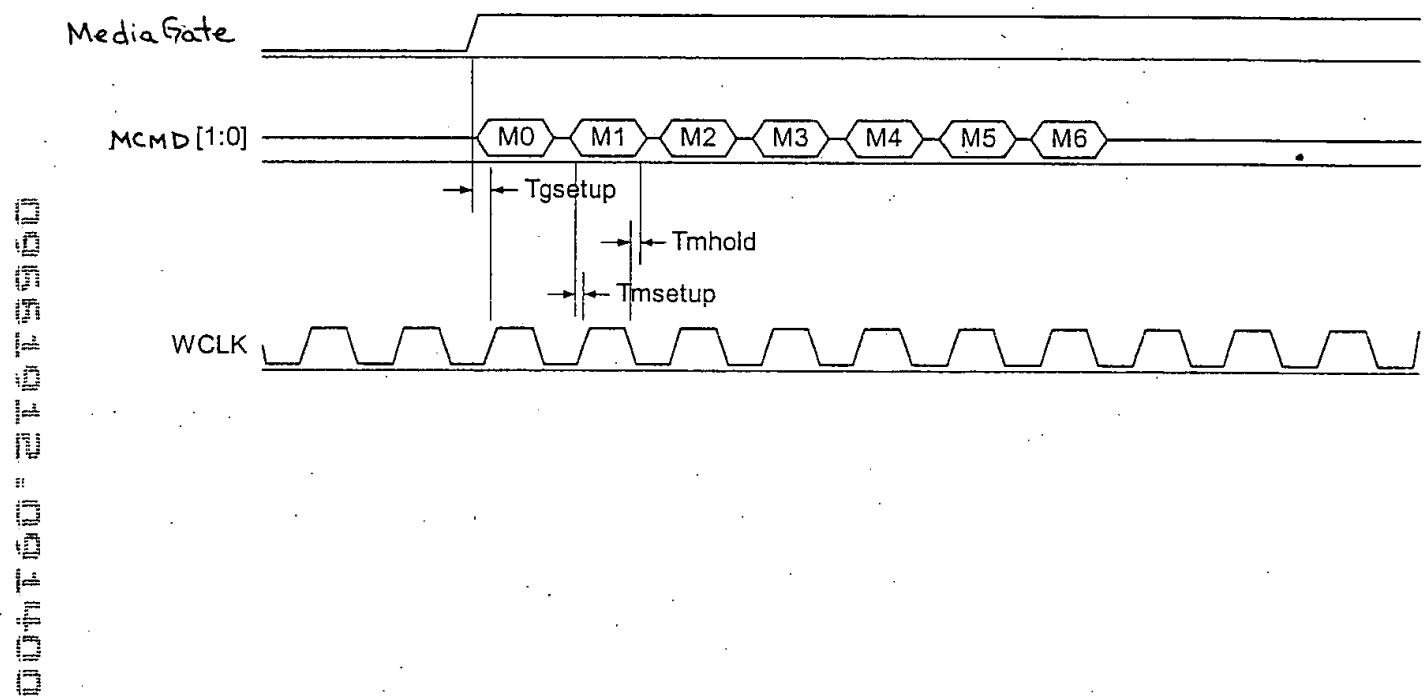
**MCMD timing chart for Write/Read operations**

Fig. 3



## High latency write

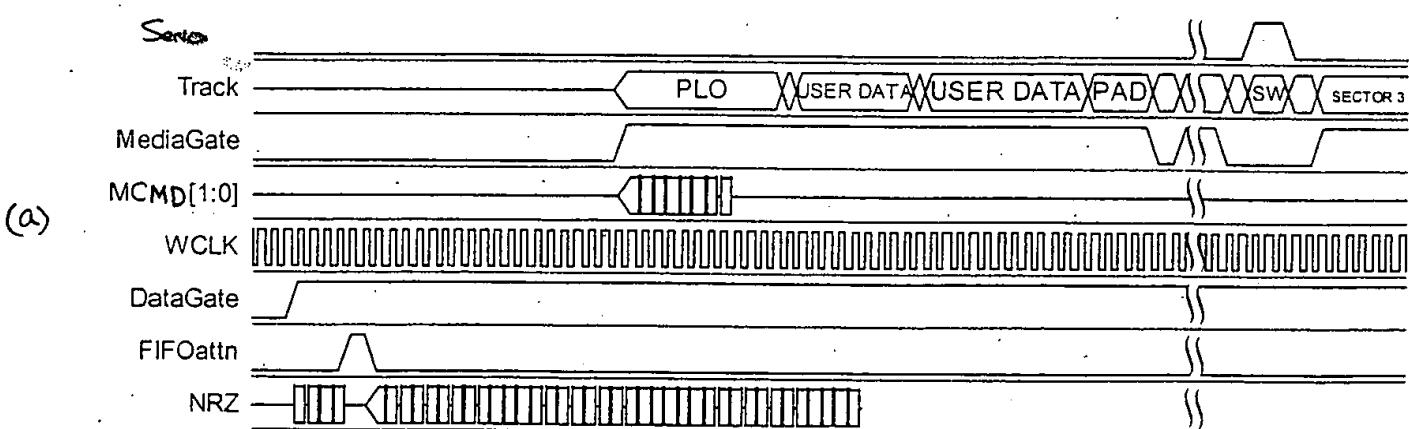
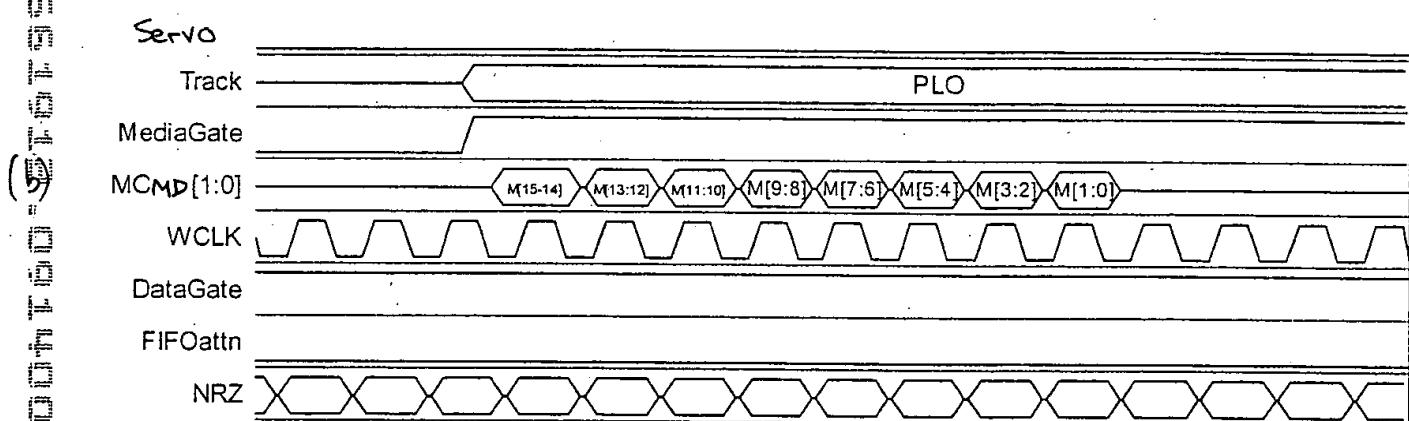
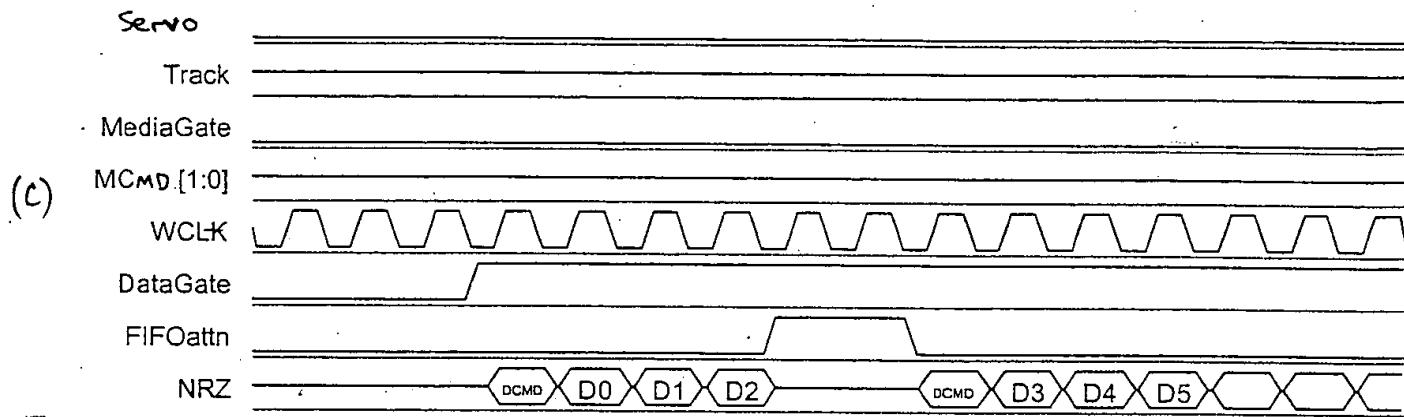
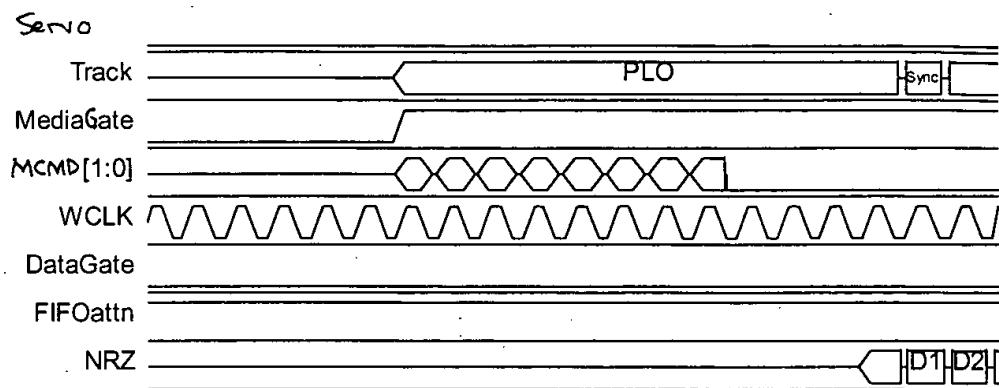


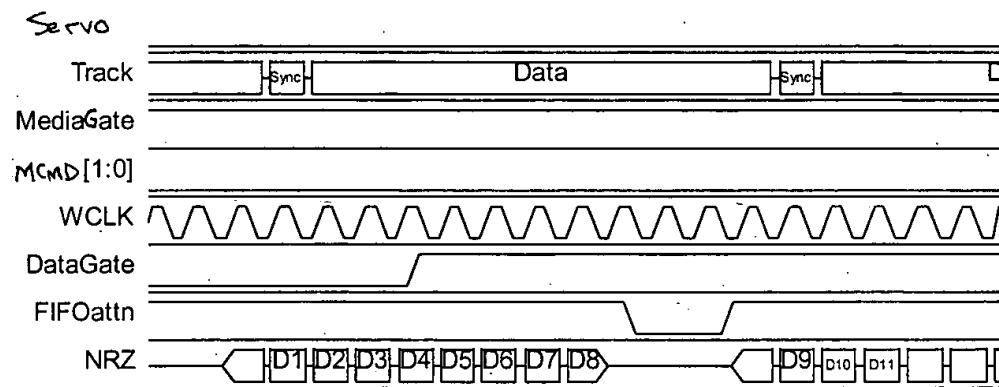
Fig. 4

DRAFT - 2016-09-06

(c)



(b)



(a)

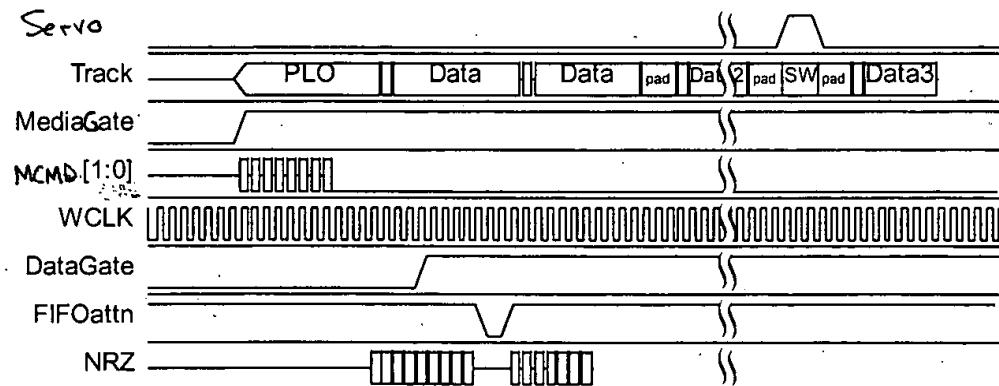


Fig. 5